The Timers

- The Traffic Signal System is based on timers - in this case four in number for each Traffic direction. At the end of all the timers, we have the final stage where we discharge all the Capacitors and reset the timing.

  Even before the 1st timer, we have 1st ASW (Alternate Switching). **refer Timing-ASW-1.png** . ASW is nothing but a NOT Gate. If no input received by the ASW, it will output a high voltage, and vice-versa. Its Q1 (a NPN) by default is OFF, and therefore the Q2 (a PNP) is ON. The Q1 would get ON only when its gets Input from the Final Stage. More on that is mentioned later in the document.

  The subsequent ASWs have been incorporated within the Timer's circuits.

- Each timer's duration is set by the RC constant logic derived from the fixed resistor, potentiometer and the Capacitor (47 uF). Please **refer Timing-1st-timer.png** .The capacitor is linked to the base of a PNP transistor (Q1). The PNP transistor's emitter is set to 2.81 V by using a voltage divider setup of 2.2 M and 1 M. therefore when the Capacitor's voltage drop increases to more than 2.81 V, the PNP transistor switches off. I had to use a low voltage drop (less than one RC Constant) in order to achieve clean and fast cut-off.

- When Q1 is ON, its signal is amplified via Q2 and Q3, and that is used to drive the load L1. Here the load is the Traffic Light Plate.

  When Q1 Switches OFF, in the 1st and the N Timer, Q5 (a PNP) switches ON which is amplified via Q6, a NPN. Transistors Q4 and Q5 are simple an ASW or a NOT Gate. The output from Q6 becomes the Input for the next timer's voltage rail. So therefore prior to Q6 switching ON, the subsequent timers and the whole chain under it is in OFF state .

  When I implemented it on the breadboard, I discovered that when a timer's voltage rail gets activated, the whole downward chain gets the current momentarily. Though it did not impact the Load of subsequent chains, but the Final Stage of the Timing Circuit, where we discharge the Capacitors, gets impacted which lead to wayward timings.

  As the last timer (**refer Timing-Last-timer-NPN-Ending.png**) is linked to the Final Stage, to make the circuit workable, I had to do a slightly different arrangement to handle the Output from the last timer which gets passed on to as the Input for the Final Stage. In the Last Timer, instead of PNP, I have used a NPN at Q5. This NPN Q5 is driven by a 10 K resistor to its base. Therefore any momentarily leakages/un-wanted currents do not get amplified enough to drive the Final stage.

- In the Final Stage (**refer Timing-Final-Stage.png**) when Q1 receive inputs, it charges the Capacitor C1 (220 uF) and we also switch off the current to the 1st Timer via 1st ASW. It is important to switch off the current to the 1st Timer as otherwise the Timer would become pre-maturely ON when discharging of capacitors is taking place. The Q2 also switches ON and all the 47 uF Capacitors of the 4 timers are also discharged.

  As all the circuits gets Switched off (including input to the Final Stage), the role of capacitor C1 becomes very important as it provides the desired current to complete the discharging process.

  When C1 gets fully discharged, the current to the 1st ASW is stopped and the 1st Timer gets switched on, thus restarting everything.

Traffic Light Set/Plate

- To handle a Traffic Light Set i.e. Red, Yellow and Green (RYG), the output L1 from the timer is set to a Pre-Amplifier (**refer Pre-RYG-Amplification.png**) for amplifying the voltage level especially around the edges of a timing section. A major problem I faced when designing this circuit was to get a clean ON and a clean OFF state

  This amplifier circuit amplifies the voltage and also we set a hight cut-off output voltage to 6.18 V using a voltage divider made of 1 M and 2.2 M resistors at the base of Q4 PNP

  This output is sent to RYG-Stage-1

- RYG-Stage-1 (**refer RYG-Stage-1.png**) - It takes Input from the Pre-RYG-Amplification stage. When there is no Input, Q1 is OFF, which in turn switches on Q2 and Q3. Output from Q3, lights Yellow of Red via OP-1 and OP-2 is sent to the AND Gate circuit for Red light.

  When there is Input, Q5 switches ON. Output from Q5, lights Yellow of Green via OP-3 and OP-4 is sent to the AND Gate circuit for Green light.

  The single Yellow light is lit momentarily via RYG-Stage-2 and the Red or Green lights are lit via RYG-Stage-3

- RYG-Stage-2 (**refer RYG-Stage-2.png**) - Both Red and Green lights have individual RYG-Stage-2 circuits. And both circuits provide output to a Single Common Yellow Light.

  The timing duration of Yellow light is determined by the RC combination of R1 (220 K) and C1 (10 uF) which is linked to the base of a PNP transistor (Q1). The PNP transistor's emitter is set to 2.81 V by using a voltage divider setup of 2.2 M and 1 M. therefore when the Capacitor's voltage drop increases to more than 2.81 V, the PNP transistor switches off. Again I had to use a low voltage drop (less than one RC Constant) in order to achieve clean and fast cut-off. With Q1 being ON, the signal is amplified via Q2 and Q3. The output OP-1 is sent to light the yellow light.

  When Q1 switches OFF, Q5 (a PNP) switches ON. Its emitter is linked to the 9V voltage rail and the output at collector is sent to the AND gate of RYG-Stage-3 of the corresponding Red or Green light. So if Q1 is ON, Q5 is OFF and vice-versa. It acts like a NOT Gate. The Output port is OP-2

- RYG-Stage-3 (**refer RYG-Stage-3.png**) - Both Red and Green lights have individual RYG-Stage-3 circuits. And both circuits provide output to light the corresponding Red or Green light.

  It is basically an AND Gate where following are ANDed
  - The Input from RYG-Stage-1 (OP-2 or OP-4, depending upon whether Red or Green)
  - The NOT output from RYG-Stage-2 - OP-2

  Therefore, Red or Green Light would not light when Yellow light is ON.

- RYG-Stage-4 (**refer RYG-Stage-4.png**)- The stage simply lights up the physical lights or LEDs